IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining lightly doped first drain and source diffusion layers;

(d) at least one sidewall covering said gate electrode therewith; and

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(e) heavily doped second drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and ~~four~~ a lateral ~~sides~~ side,

said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a horizontal surface of said semiconductor substrate in at least one of regions below which at least one of said second drain and source diffusion layers are to be formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a ~~vertical~~ thickness of ~~said lateral surface of~~ said sidewall,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset, and at least one of said drain and source diffusion layers extending no closer to said gate electrode than said edge of said sidewall offset.

2. (Original) The semiconductor device as set forth in claim 1, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

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3. (Original) The semiconductor device as set forth in claim 1, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

4. (Original) The semiconductor device as set forth in claim 3, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

5. (Original) The semiconductor device as set forth in claim 1, further comprising a memory cell formed on said semiconductor substrate.

6. (Currently amended) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining lightly doped first drain and source diffusion layers;

(d) at least one sidewall covering said gate electrode therewith;

(e) heavily doped second drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and ~~four~~ a lateral ~~sides~~ side,

said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a horizontal surface of said semiconductor substrate in at least one of regions below which at least one of said second drain and source diffusion layers are formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a ~~vertical~~ thickness of ~~said lateral surface of~~ said sidewall; and

(f) low-resistive wiring layers formed at surfaces of said drain and source diffusion layers, said low-resistive wiring layers being located outwardly beyond

a peripheral edge of at least one of said sidewall and said sidewall offset in said at least one of said drain and source diffusion layers,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset, and at least one of said drain and source diffusion layers extending no closer to said gate electrode than said edge of said sidewall offset.

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7. (Original) The semiconductor device as set forth in claim 6, wherein said low-resistive wiring layers are composed of TiSi.

8. (Original) The semiconductor device as set forth in claim 6, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

9. (Original) The semiconductor device as set forth in claim 6, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

10. (Original) The semiconductor device as set forth in claim 9, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

11. (Original) The semiconductor device as set forth in claim 6, further comprising a memory cell formed on said semiconductor substrate.

Claims 12-19. (Cancelled)

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20. (Currently amended) The semiconductor device of Claim 1, wherein said sidewall offset extends in only one direction towards ~~one of~~ said source and drain diffusion layers.

21. (Currently amended) The semiconductor device of Claim 1, wherein said sidewall entirely covers said gate electrode.

22. (Currently amended) The semiconductor device of Claim 6, wherein said sidewall offset ~~in said at least one of said drain and source diffusion layers~~ extends in only one direction from said gate electrode towards ~~one of~~ said source and drain diffusion layers~~, the other of said at least one of said drain and source diffusion layers having no sidewall offset~~.

23. (Currently amended) The semiconductor device of Claim 6, wherein said sidewall entirely covers said gate electrode.